Joint Undervolting and Overclocking Power Scaling Approximation on FPGAs

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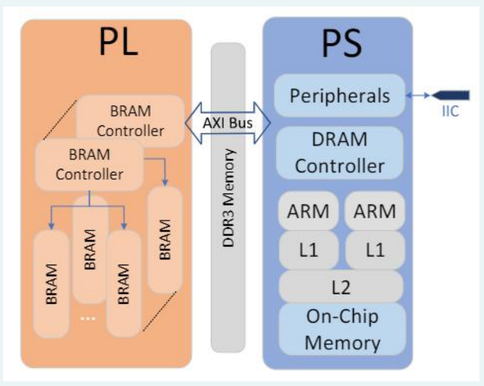
Motivation:

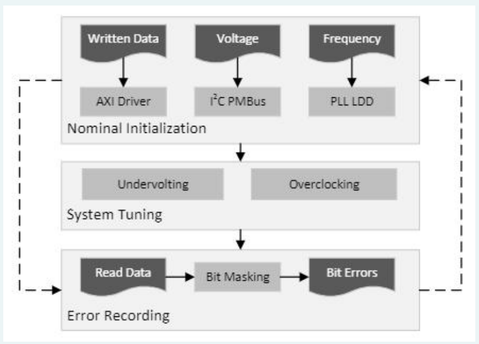
- Assume we have designed an FPGA accelerator, e.g. using sensible arithmetic approximation
- Research Question: Can I reduce the supply voltage and overclock to reduce power and improve the energy efficiency?

Hardware infrastructure



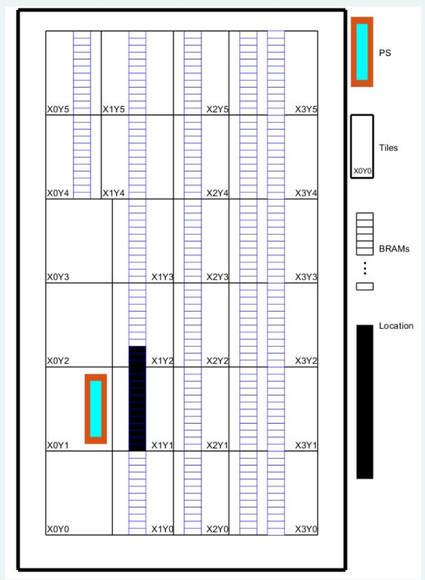
Datapath. Size (KB)	Reg.	LUT	BRAM	Address	Frequency (MHz)
4	3954	3160	1	0x0-0xFFF	100
16	3974	3171	4	0x0-0x3FFF	100
32	3984	3177	8	0x0-0x7FFF	100
64	3994	3175	16	0x0-0xFFFF	100
128	4004	3191	32	0x0-0x1FFFF	100

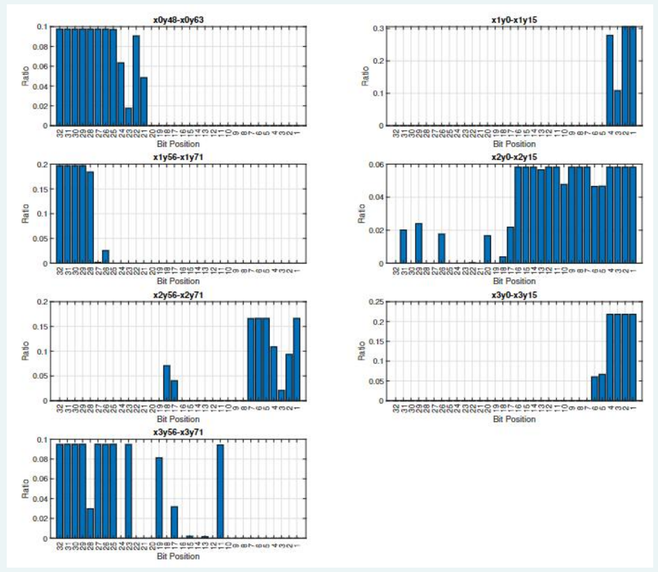
Software infrastructure

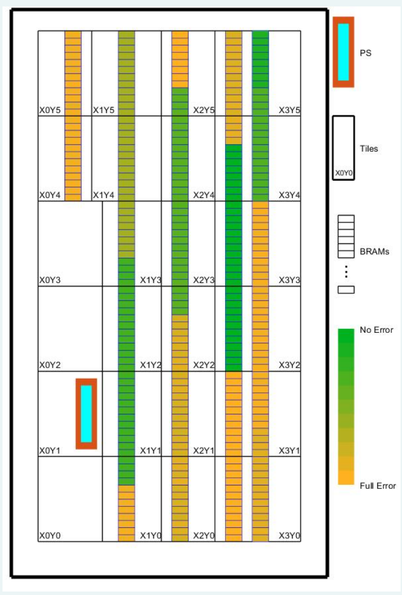


Case No.	Patterns (64 Bits)
c1	0x00000000 / 0xFFFFFFFF
c2	0xFFFF0000 / 0x0000FFFF
c3	0xFF00FF00 / 0x00FF00FF
c4	0xF0F0F0F0 / 0x0F0F0F0F
c5	0x33333333 / 0xCCCCCCCC
c6	0x55555555 / 0xAAAAAAAA

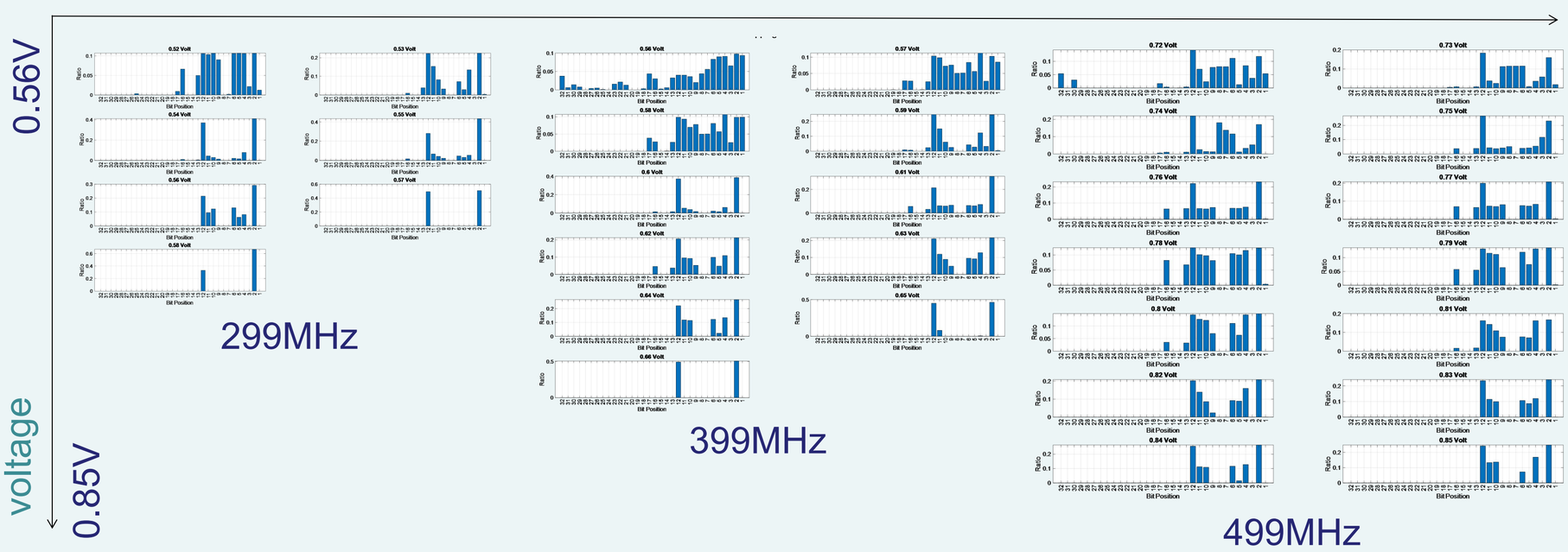
Approximate Location



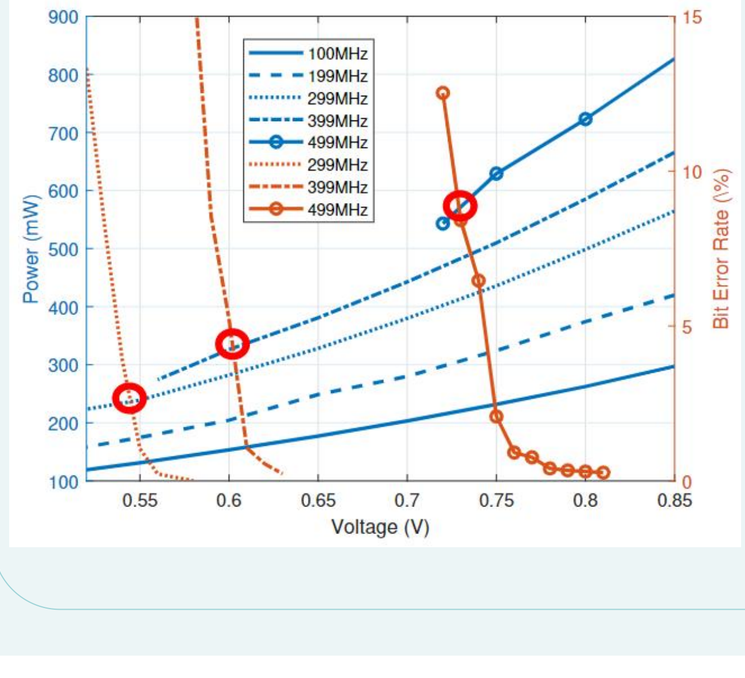


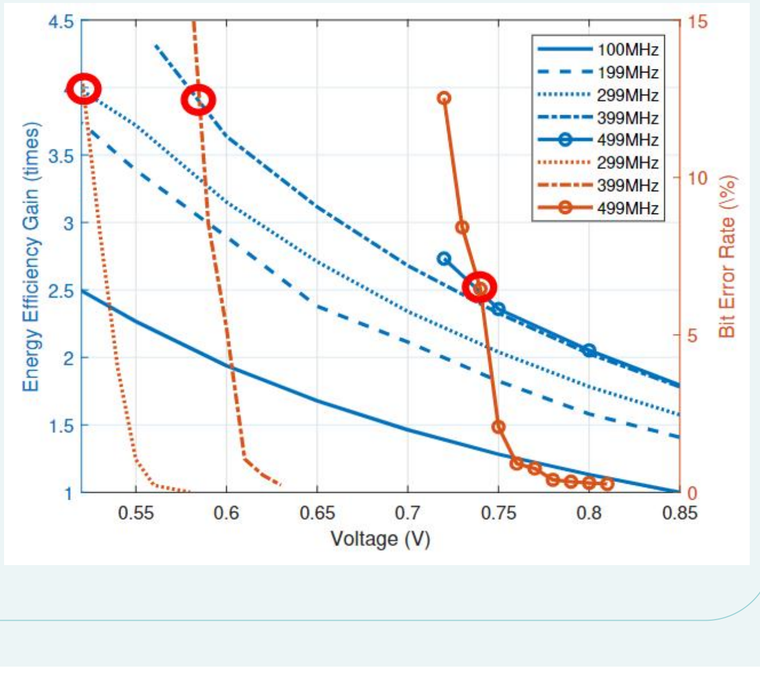


Approximate Datapath



Power & energy v.s. bit error rate against voltage & frequency





Conclusions:

- Yes, further substantial improvements are feasible
- Up to ~60% power saving
- At least ~2.5x energy efficiency
- Bit-flipping error patterns are device and location dependent

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